WINCHESTER DISK INTERFACE PCB FOR THE PERIPHERAL EXPANSION SYSTEM

SPEC DWG. #JPM0002

7/23/82

SECTION 1

WINCHESTER DISK INTERFACE ELECTRICAL DEFINITION

1.1 ORGANIZATION

The Winchester Disk I/F PCB shall be an interface between the TI 99/4A or LCP mainframe and a XEBEC S1410 or Shugart S1410/1420A Winchester Disk Controller. The Winchester Disk I/F PCB will be located in the TI 99/4 Peripheral Expansion System. The Winchester Disk Controller will be located in a single enclosure with the TI 5-1/4" Winchester Disk Drive and an adequate power supply. A single 50-conductor ribbon cable will be the only connection necessary between the PES and the Winchester Disk Subsystem. The Disk Controller shall be capable of driving a minimum of 2 Winchester Disk Drives. The second Winchester Disk Drive shall not need a controller board.

1.2 GENERAL

* There shall be no more than one input connected to the System driven Bus. No more than three open collector or tri-state outputs may be connected to drive the System Bus. Both bus drivers and receivers shall be physically located close to the System I/O connector.

* Memory/CRU space decodes shall comprehend PLA decoding as a cost reduction path.

* Adequate decoupling shall be provided on the logic and the output drivers.

1.3 KNOWN 99/4A TO LCP INCOMPATIBILITIES

None known at this time.

1.4 TEST CONSIDERATIONS

Signature Analysis shall be designed in as the primary fault isolation tool, and test specifications for this PCB shall written after both design and prototype debug have been completed.

1.5 LED INDICATOR

A single LED shall be provided that is under Software Control. The exact operation of this LED shall be determined later. As currently defined, the LED shall be on whenever the DSR ROM is enabled.

1.6 DSR ROM

The DSR ROM space decode shall be a function of the 19 System Address lines, MEMEN*, DBIN, and the signal PCBEN. PCBEN is a HIGH true signal that will be used in the Burn In Racks.

The DSR ROM shall be considered to be a 12K x 8 ROM, and shall be decoded to respond to >74000 to >74DEF and >75000 to >75FFF(>4000 to >4DEF and >5000 to > 5FFF for the 99/4A) only. It shall also be connected such that an EPROM can be substituted with no wiring changes.

The 12K DSR ROM space shall support a 4K by 8 ROM(or EPROM) and a 8K by 8 ROM(or EPROM). The 4K ROM shall occupy the >4000 to >4DEF space, with the >4E00 to >4FFF being used by the header RAM(>4E00 to >4EFF) and the sector buffer RAM(>4F00 to >4FFF). The 8K by 8 ROM(or EPROM) shall occupy the >5000 to >5FFF space, with a single CRU bit used to select between the two 4K pages.

The DSR ROM base address shall be at >74000 (>4000 for the 99/4A). The DSR ROM Page enable for the Winchester Disk I/F board shall respond to a CRU base of >01000(>1000 for the 99/4A).

1.7 INTERFACING TO THE WINCHESTER DISK CONTROLLER

The Winchester Disk Controller shall be memory mapped at an address of >74DX (>4BFX for the 99/4A). The Winchester Disk controller requires only a single memory mapped byte for data. Three(3) control lines are driven by the Winchester Disk I/F PCB and five(5) are received. All received control lines shall be

able to be monitored by CRU to aid in debug, fault isolation, etc. However, some of the control lines will be controlled automatically by on-board logic during hardware memory transfer. Also, all control lines driven by the Winchester Disk I/F PCB shall be capable of being controlled by CRU(the ACK/ line can also be controlled by the on board logic during memory transfer).

1.8 HARDWARE MEMORY READ/WRITE

The Winchester Disk I/F PCB shall be able to transfer data to/from a 256 byte block of on board RAM to/from the Winchester Disk Controller. This hardware read/write shall be initiated by setting a single CRU output bit high and immediately setting it back low. The system READY line shall not be held false during this transfer, but a CRU bit shall be set upon completion.

* NOTE: Only the actual memory data from the selected 256 byte block of Sector Buffer RAM will be transferred automatically. All overhead information MUST be transferred by directly writing to the Winchesters memory mapped address. The Header Buffer RAM is used by the CPU as a remote storage for the overhead data normally stored in the CPU RAM.

If an timeout error occurs during this data transfer, a single CRU input bit shall be set, for testing by software.

1.9 STATE COUNTER

A state counter shall be used to control the hardware memory read/write. This state counter shall be initialized during power-up reset and shall idle waiting for the SBO,SBZ combination of the CRU bit used to signal the state counter to start the sector dump.

1.10 CRU DEFINITION

The CRU space shall comprehend 15 System Address lines (the most significant three of the 99/4B shall be assumed to be zeros), MEMEM*, and the HIGH true signal PCBEN which will be used in the Burn In Racks. CRU addresses for the 99/4A are derived from LCP addresses by dropping the most significant character (3 bits).

* The CRU base address for the Winchester Disk I/F PCB shall be at >01000, and the DSR ROM Page enable shall respond to a CRU address of >01000.

* A System RESET shall set the DSR ROM page bit to a state that disables the DSR ROM.

1.10.1 LED Indicator Bit. A single output bit shall be used to drive the Indicator LED, and the operation of this LED shall be determined later.

1.10.2 Eight K ROM Page. A single CRU output bit shall be used as a page select for the 8K ROM located at >5XXX.

1.10.3 Hardware Read/Write. A single output bit shall be used to configure the Winchester Disk I/F PCB to automatically read into or write from a 256-Byte block of on-board RAM.

1.10.4 Start Hardware Dump. A single CRU output bit shall be used to start a hardware dump of memory. The direction of the data flow is determined by another CRU output bit previously defined.

1.10.5 Header RAM Block Select. Two CRU output bits shall be used to select 1 of 4 256-Byte blocks of available 1K Header RAM is mapped into the >4E00 to >4EFF address space.

1.10.6 Sector Buffer RAM Block Select. Four CRU bits shall be used to select 1 of 16 256-Byte Sector Buffers of available 4K RAM to be mapped in the >4F00 to >4FFF address space.

1.10.7 Timeout Error. A single CRU input bit shall be used to signal the CPU that a timeout error occured during a hardware dump.

1.10.8 CRU Bit Definitions.

Output Bit Displacement	Definition
0	DSR ROM Page Enable, 1 = enabled
1	Sector buffer RAM block select ,LSB
2	Sector buffer RAM block select
3	Sector buffer RAM block select
4	Sector buffer RAM block select ,MSB
5	Header RAM block select LSB
6	Header RAM block select MSB
7	Data direction during hardware dump, 0 = from I/F PCB to Disk, 1 = from Disk to I/F PCB.
8	DRVSEL, Winchester Drive Select, 1 => Selected
9	DRVRST, Winchester Drive Reset, 1 => Reset Drive
10	EKRPG, selects page of 8K ROM @ >5XXX
11	DMPENA, Start Hardware dump

Input Bit Displacement	Definition
0 (Qualified by REQ)	I/O*, Controller driven, 0 = from Controller to Host 1 = from Host to controller
1 (Qualified by REQ)	C/D*, Controller driven, 0 = Data Bytes 1 = Control Bytes
2 (Qualified by REQ)	MSG, Controller Driven, 0 = Command is being execut 1 = Command Completed
3	BSY, Controller Driven, 0 = Controller not selected 1 = Controller selected & Ready
4	REQ, Controller Driven Handshake 1 = I/O*, C/D*, MSG are Qualified
5	SPARE
6	SPARE
7	Timeout Error during Hardware Dump

1.11 INTERRUPTS

The interrupt from the Winchester Disk shall drive Interrupt Level A (ILA*). Interrupt Level Status Bit (ILSB) 0 shall be driven for the Winchester Disk interrupt and be used on the 99/4B, but the Johnny Box shall not use interrupts. The ILSA* shall be gated to the Data Bus with the LOW true signal

"SENILB*".

1.12 FLAGS

Where practical, all unused CRU input bits shall be connected to unused output bits to form flag bits.

1.13 I/O VOLTAGE LEVELS

All System Bus signals shall comply with standard TTL voltage levels.

1.13.1 Connectors. The Winchester Disk Interface connector shall accept a 50-position female ribbon cable connector, AMP _____-_ or equivalent, and shall conform to the pin definitions that are listed under I/O PORT DEFINITION.

1.14 PAL EQUATION DEFINITIONS

The following are the equations necessary for programming the PAL.

PAL 1

```
/FKROM = V10*/V11*A1*/A3*PCBEN*DBIN*MEMEN*/A4                    (4000-47FF)
        +V10*/V11*A1*/A3*PCBEN*DBIN*MEMEN*/A6*/A7                (44XX, 48XX, 4CXX)
        +V10*/V11*A1*/A3*PCBEN*DBIN*MEMEN*A4*A5*/A6*A7*/V12      (4D00-4DEF)
        +V10*/V11*A1*/A3*PCBEN*DBIN*MEMEN*A4*/A5                 (4800-4BFF)

/EKROM = V10*/V11*A1*A3*PCBEN*DBIN*MEMEN*/A4                     (5000-5FFF)

/FKRAM = V10*/V11*A1*/A3*PCBEN*MEMEN*A1*/A3*A4*A5*A6*A7          (4F00-4FFF)

/OKRAM = V10*/V11*A1*/A3*PCBEN*MEMEN*A1*/A3*A4*A5*A6*/A7         (4E00-4EFF)

/HDSKEN= V10*/V11*A1*/A3*PCBEN*MEMEN*A1*/A3*A4*A5*/A6*A7*V12     (4E00-4EFF)

/CRUEN = PCBEN*/MEMEN*/V11*/A1*A3*/A4*/A5*/A6*/A7                (1000-10FF)

        V10 = AMA*AMB*AMC*RPGEN
        V11 = A00 + A02
        V12 = A08*A09*A10*A11
```

PAL 2

```
/BDRVR = MEMEN*V20*/V11*A1                                       (4000-5FFF)

/FKRWE = /DMPENA*WE + DMPENA*DMPDIR*RAMR/W

/FKROE = /DMPENA*DBIN + DMPENA*/DMPDIR

/I/OLTCH = /DMPENA*HDSKEN + /DMPENA*/WE + DMPENA*/ACK

/I/ORD = DMPENA*I/O- + /DMPENA*HDSKEN*DBIN
```

WINCHESTER-DISK I/O PORT DEFINITION

PIN	TYPE	SIGNAL	FUNCTION
1		GROUND	
2	I/O	DATA0/	Data Bus, Bit 0(LSB)
3		GROUND	
4	I/O	DATA1/	Data Bus, Bit 1
5		GROUND	
6	I/O	DATA2/	Data Bus, Bit 2
7		GROUND	
8	I/O	DATA3/	Data Bus, Bit 3
9		GROUND	
10	I/O	DATA4/	Data Bus, Bit 4
11		GROUND	
12	I/O	DATA5/	Data Bus, Bit 5
13		GROUND	
14	I/O	DATA6/	Data Bus, Bit 6
15		GROUND	
16	I/O	DATA7/	Data Bus, Bit 7(MSB)
17		GROUND	
18		SPARE	
19		GROUND	
20		SPARE	
21		GROUND	
22		SPARE	
23		GROUND	
24		SPARE	
25		GROUND	
26		SPARE	
27		GROUND	
28		SPARE	
29		GROUND	
30		SPARE	
31		GROUND	
32		SPARE	
33		GROUND	
34		SPARE	
35		GROUND	
36	received	BUSY/	Controller is ready
37		GROUND	
38	driven	ACK/	Response to REQ/
39		GROUND	
40	driven	RST/	Reset Controller
41		GROUND	
42	received	MSG/	Command completed
43		GROUND	
44	driven	SEL/	Select Controller
45		GROUND	
46	received	C/D	Command/Data

47		GROUND	
48	received	REQ/	Request(start hndshk)
49		GROUND	
50	received	I/O	Input/Output(dir of DIO)

System Bus I/O Connector Pin Definition
.100" PIN TO PIN SPACING, PRODUCTION PCBS

PIN #	MNEMONIC	FUNCTION
1		+12V 3-T Regulator supply voltage
2		+12V 3-T Regulator supply voltage
XX		-12V 3-T Regulator supply voltage
XX		-12V 3-T Regulator supply voltage
3	GND	Logic Ground
5	GND	Logic Ground
6	RESET*	active LOW System driven RESET
7	GND	Logic Ground
11	BDRVREN*	Enable for I/F card buffers
12	PCBEN	active HIGH PCB enable for Burn In
13	HOLD*	Active LOW CPU HOLD request Available on LCP only
14	IAQHDA	IAQ HOLDA Logical OR Available on LCP only
C(15	SENILA*	Interrupt Level A Sense Enable)
16	SENILB*	Interrupt Level B Sense Enable Used on LCP only
17	INTA*	active LOW Interrupt Level A
18	INTB*	active LOW Interrupt Level B used on LCP only
19	D7	System DATA Bus, LSB
20	GND	Logic Ground
21	D5	System DATA Bus
22	D6	System DATA Bus
23	D3	System DATA Bus
24	D4	System DATA Bus
25	D1	System DATA Bus
26	D2	System DATA Bus
27	GND	Logic Ground
28	D0	System DATA Bus, MSB
29	A14.A	Address Bit
30	A15/COUT.A	Address Bit, LSB
31	A12.A	Address Bit
32	A13.A	Address Bit
33	A10.A	Address Bit
34	A11.A	Address Bit
35	A08.A	Address Bit
36	A09.A	Address Bit
37	A06.A	Address Bit
38	A07.A	Address Bit
39	A04.A	Address Bit
40	A05.A	Address Bit

PRODUCTION PCB PIN OUTS, CONTINUED

PIN #	MNEMONIC	FUNCTION
41	A02.A	Address Bit
42	A03.A	Address Bit
43	A00.A	Address Bit, (MSB, Johnny Box)
44	A01.A	Address Bit
45	AMB.A	Address Bit
46	AMA.A	Address Bit
48	AMC.A	Address Bit, (MSB, 99/4B)
XX		not used, INTA*
XX		not used, SENILA*
XX		not used, HOLD*
XX		not used, IAQHDA
XX		not assigned
XX		not used, BOOTPG*
XX		not used, AUDIO
47	GND	Logic Ground
XX		not used, SCLK
49	GND	Logic Ground
50	CLKOUT*	Active LOW CPU Clock
51	CRUCLK.A*	active LOW CRU Output Clock
52	DBIN.A	Data Bus Dir'tn, HIGH is CPU READ
53	GND	Logic Ground
54	WE.A*	LOW true CPU Write Enable
55	CRUIN	HIGH true CRU Input data
56	MEMEN.A*	active LOW memory request
XX		not used, READY.A
59		+5V 3-T Regulator supply voltage
60		+5V 3-T Regulator supply voltage

1.15 MNEMONIC DEFINITIONS

MNEMONIC	DEFINITION
AMC.A	System 19-bit Address Bus MSB
AMB.A	System 19-bit Address Bus
AMA.A	System 19-bit Address Bus
A00.A	System 19-bit Address Bus

A01. A	System 19-bit Address Bus
A02. A	System 19-bit Address Bus
A03. A	System 19-bit Address Bus
A04. A	System 19-bit Address Bus
A05. A	System 19-bit Address Bus

MNEMONIC	DEFINITION
A06.A	System 19-bit Address Bus
A07.A	System 19-bit Address Bus
A08.A	System 19-bit Address Bus
A09.A	System 19-bit Address Bus
A10.A	System 19-bit Address Bus
A11.A	System 19-bit Address Bus
A12.A	System 19-bit Address Bus
A13.A	System 19-bit Address Bus
A14.A	System 19-bit Address Bus
A15/COUT.A	System combination Address Bus LSB and CRU Output Data.
AMC.B	Buffered 19-bit Address Bus MSB
AMB.B	Buffered 19-bit Address Bus
AMA.B	Buffered 19-bit Address Bus
A00.B	Buffered 19-bit Address Bus
A01.B	Buffered 19-bit Address Bus
A02.B	Buffered 19-bit Address Bus
A03.B	Buffered 19-bit Address Bus
A04.B	Buffered 19-bit Address Bus
A05.B	Buffered 19-bit Address Bus
A06.B	Buffered 19-bit Address Bus
A07.B	Buffered 19-bit Address Bus
A08.B	Buffered 19-bit Address Bus

MNEMONIC	DEFINITION
A09.B	Buffered 19-bit Address Bus
A10.B	Buffered 19-bit Address Bus
A11.B	Buffered 19-bit Address Bus
A12.B	Buffered 19-bit Address Bus
A13.B	Buffered 19-bit Address Bus
A14.B	Buffered 19-bit Address Bus
A15/COUT.B	Buffered combination 19-bit Address Bus LSB and CRU Output Data.
BDRVR*	Active Low enable for the Data Bus Bidirectional Bus driver chip (SN74LS245).
CLKOUT.A*	Bus level System Clock. For 99/4A based systems it is the 3 MHz Phase 3 clock. For 99/4B based systems it is a 2.68 MHz clock similiar to a 99/4A, but more than twice as wide and a different frequency.
CLKOUT.B*	Buffered System Clock. For 99/4A based systems it is the 3 MHz Phase 3 clock. For 99/4B based systems it is a 2.68 MHz clock similiar to a 99/4A, but more than twice as wide and a different frequency.
CRUCLK.A*	System level, Active LOW CRU Clock from the CPU.
CRUCLK.B	Buffered, Active HIGH CRU Clock from the CPU.
CRUCLK.B*	Buffered, Active Low CRU Clock from the CPU.
CRUIN	High True CRU data to the CPU (CRU READ Data).
CRUO*	Active Low enable for a bit CRU operation. It is the CRU base of >01D00

MNEMONIC	DEFINITION
DBIN.B	Buffered, Active Low Data Bus Input control line. The data direction is from the PCB to the CPU when this line is HIGH.
DBIN.B*	Buffered Active Low Data Bus Input control line. The data direction is from the PCB to the CPU when this line is LOW.
DSRROM*	Active Low DSR ROM enable to be ANDed with DBIN.B to drive the DSR ROM Chip Enable pin.
D0	System Side Data Bus MSB
D1	System Side Data Bus
D2	System Side Data Bus
D3	System Side Data Bus
D4	System Side Data Bus
D5	System Side Data Bus
D6	System Side Data Bus
D7	System Side Data Bus LSB
IFC	Interface Clear, sent by the system controller to set the system into a known quiescent state. The system controller becomes the controller in charge.

MNEMONIC	DEFINITION
ILB*	Tristate, Active Low driver for Interrupt Level B.
MEMEN. A*	System Memory Enable control signal from the CPU. When LOW it indicates that a memory access IS required by the CPU. When HIGH it indicates that a CRU MIGHT be taking place.
MEMEN. B*	Buffered Memory Enable control signal from the CPU. When LOW it indicates that a memory access IS required by the CPU. When HIGH it indicates that a CRU MIGHT be taking place.
PCBEN	Active High PCB enable signal. It is used on the Burn In Rack to allow the controlling CPU to talk to only one PCB at a time. When LOW the PCB is disabled for both CRU and Memory operations.

MNEMONIC	DEFINITION
RD0	PCB Side Data Bus MSB
RD1	PCB Side Data Bus
RD2	PCB Side Data Bus
RD3	PCB Side Data Bus
RD4	PCB Side Data Bus
RD5	PCB Side Data Bus
RD6	PCB Side Data Bus
RD7	PCB Side Data Bus LSB
RESET.A*	System Active Low Master Reset line form the CPU.
RESET.B*	Buffered Active Low Master Reset line form the CPU.
RPGEN	Active High DSR ROM Page Bit. It must be HIGH before the DSR ROM may be accessed.
SENILB*	CPU driven line to allow the PCB to gate interrupt data to the system side of the Data Bus.

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SECTION 1

INTRODUCTION

1.1 SCOPE

This document describes the electrical, environmental, documentation, and system software requirements for the TI Winchester Disk Subsystem for the 99/X series Home Computer).

SECTION 2

APPLICABLE DOCUMENTS

* SMALL COMPUTER SYSTEM INTERFACE(SCSI) - ANSI X3T9.2/82-2
* TI-99/4A CONSOLE AND PERIPHERAL EXPANSION SYSTEM TECHNICAL DATA MANUAL(1049717-1)
* FCC DOCKET 20780
* NATIONAL SAFE TRANSIENT PRESHIPMENT TEST PROCEDURE
* ORAS 16237
* MIL STD 810B, 461, 462

SECTION 3

FUNCTIONAL HARDWARE DESCRIPTION

3.1 SCOPE

The TI Winchester Disk Subsytem for the 99/X Series of Home Computers consists of a TI 5-1/4" Winchester Drive(6 MByte or 12 MByte), a SCSI-compatible Winchester drive controller, power supply, and a suitable enclosure. This subsystem shall interface to the 99/X Computer through a Host Adaptor boardthat resides in the Peripheral Expansion System.

3.2 HOST ADAPTOR BOARD

The SCSI Host Adaptor PCB shall provide the neccesary logic to convert the TI Expansion System Bus to SCSI standards. In addition, this PCB shall provide the following:

* 12K x 8 Device Service Routine(DSR) ROM
* 1K x 8 File Header Storage RAM
* 4K x 8 Sector Buffer RAM
* Logic to transfer 1-256 Byte Sector between the Host Adaptor and the SCSI Bus port
* LED Indicator
* SCSI Bus compatible drivers/receivers

3.2.1 DESIGN RULES.

* There shall be no more than one input connected to the System driven Bus. No more than three open collector or tri-state outputs may be connected to drive the System Bus. Both bus drivers and receivers shall be physically located close to the System I/O connector.
* Memory/CRU space decodes shall comprehend PLA decoding

as a cost reduction path.

* Adequate decoupling shall be provided on the logic and the output drivers.

3.2.2 Memory Map.

3.2.2.1 DSR ROM. The DSR ROM space decode shall be a function of the 19 System Address lines, MEMEN*, DBIN, and the signal PCBEN. PCBEN is a HIGH true signal that will be used in the Burn In Racks.

The DSR ROM shall be considered to be a 12K x 8 ROM, and shall be decoded to respond to >74000 to >74DEF and >75000 to >75FFF(>4000 to >4DEF and >5000 to >5FFF for the 99/4A) only. It shall also be connected such that an EPROM can be substituted with no wiring changes.

The 12K DSR ROM space shall support a 4K by 8 ROM(or EPROM) and an 8K by 8 ROM(or EPROM). The 4K ROM shall occupy the >4000 to >4DEF space, with the >4E00 to >4FFF being used by the header RAM(>4E00 to >4EFF) and the sector buffer RAM(>4F00 to >4FFF). The 8K by 8 ROM(or EPROM) shall occupy the >5000 to >5FFF space, with a single CRU bit used to select between the two 4K pages.

The DSR ROM base address shall be at >74000 (>4000 for the 99/4A). The DSR ROM Page enable for the SCSI Host Adaptor I/F board shall respond to a CRU base of >01000(>1000 for the 99/4A).

3.2.3 Interfacing to the SCSI Port. The SCSI Bus port shall be memory mapped at an address of >74BFF (>4BFF for the 99/4A). The SCSI Bus port requires only a single memory mapped byte for data. Three(3) control lines are driven by the Host Adaptor PCB and five(5) are received. All received control lines shall be able to be monitored by CRU to aid in debug, fault isolation, etc. Also, all control lines driven by the Host Adaptor PCB shall be capable of being controlled by CRU(the ACK/ line can also be controlled by the on board logic during memory transfer).

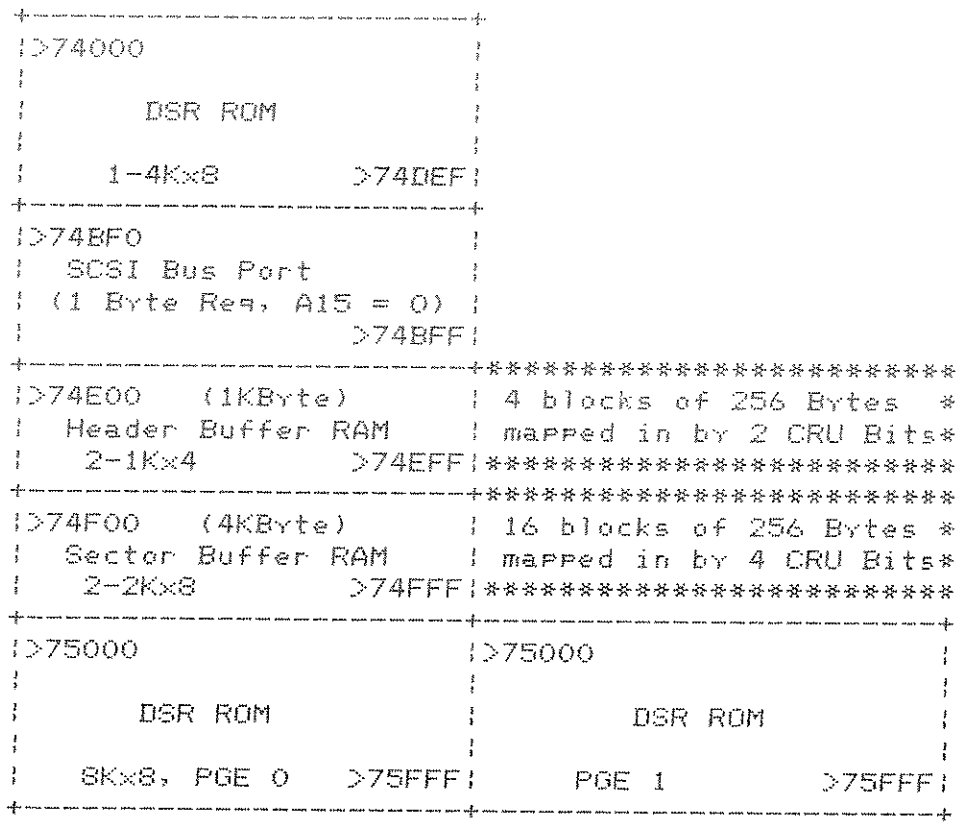
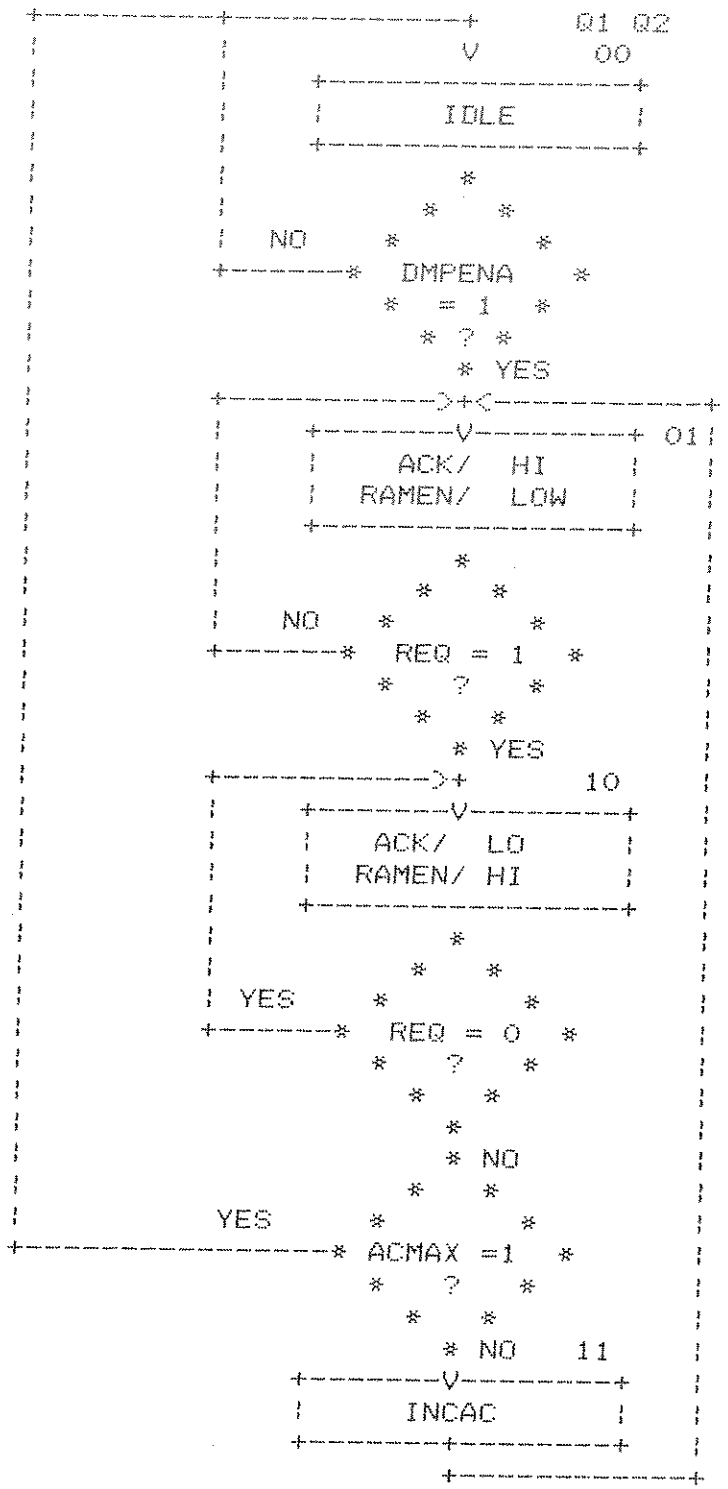


Figure 3-1 MEMORY MAP OF SCSI HOST APAPTOR PCB

3.2.4 Hardware Memory Read/Write. The SCSI Host Adaptor PCB shall be able to transfer data to/from a 256 byte block of on board RAM to/from the SCSI Bus port. This hardware read/write shall be initiated by setting a single CRU output bit high and immediately setting it back low. The system READY line shall not be held false during this transfer, but a CRU bit shall be set upon completion.

* NOTE: Only the actual memory data from the selected 256 byte block of Sector Buffer RAM will be transferred automatically. All overhead information MUST be transferred by directly writing to the SCSI Bus ports memory mapped address. The Header Buffer RAM is used by the CPU as a remote storage for the overhead data normally stored in the CPU RAM.

3.2.5 State Counter. A state counter shall be used to control the hardware memory read/write. This state counter shall be initialized during power-up reset and shall idle waiting for the SBO,SBZ combination of the CRU bit used to signal the state counter to start the sector dump.



Fisure 3-2 HARDWARE SECTOR READ/WRITE FLOW CHART

3.2.6 LED Indicator. As currently defined, the LED on the Host Adaptor card that resides in the Expansion System shall be on whenever the DSR ROM is enabled.

3.2.7 CRU Definition. The CRU space shall comprehend 15 System Address lines (the most significant three of the Armadillo shall be assumed to be zeros), MEMEM*, and the HIGH true signal PCBEN which will be used in the Burn In Racks. CRU addresses for the 99/4A are derived from Armadillo addresses by dropping the most significant character (3 bits).

* The CRU base address for the SCSI Host Adaptor PCB shall be at >01000, and the DSR ROM Page enable shall respond to a CRU address of >01000.

* A System RESET shall set the DSR ROM page bit to a state that disables the DSR ROM and set the state counter to an idle state.

3.2.7.1 Page Enable. The Page Enable bit shall be at CRU offset 0 and shall enable the 4K DSR ROM and the on-board LED.

3.2.7.2 Eight K ROM Page. A single CRU output bit shall be used as a page select for the 8K ROM located at >5XXX.

3.2.7.3 Hardware Read/Write. A single output bit shall be used to configure the SCSI Host Adaptor PCB to automatically read into or write from a 256-Byte block of on-board RAM. Power-up value shall be to read from the SCSI Bus port to prevent possible data transmission to the SCSI.

3.2.7.4 Start Hardware Dump. A single CRU output bit shall be used to start a hardware dump of memory. The direction of the data flow is determined by the Hardware R/W bit previously defined. This bit must be set HI to start the dump, and must be set low before the state counter is through(~ 2 usec min.).

3.2.7.5 Header Block RAM Select. Two CRU output bits shall be used to select 1 of 4 256-Byte blocks of available 1K Header RAM is mapped into the >4E00 to >4EFF address space.

3.2.7.6 Sector Buffer RAM Block Select. Four CRU bits shall be used to select 1 of 16 256-Byte Sector Buffers of available 4K RAM to be mapped in the >4F00 to >4FFF address space.

Output Bit Displacement	Definition
0	RPGEN: DSR ROM Page Enable, 1 = enabled
1	RA0: Sector buffer RAM block select ,LSB
2	RA1: Sector buffer RAM block select
3	RA2: Sector buffer RAM block select
4	BNKSEL: Sector buffer RAM block select ,MSB
5	RR0: Header RAM block select LSB
6	RR1: Header RAM block select MSB
7	DMPDIR: Data direction during hardware dump, 0 = from I/F PCB to Disk, 1 = from Disk to I/F PCB.
8	DRVSEL: SCSI Device Select, 1 => Selected
9	DRVRST: SCSI Device Reset, 1 => Reset Drive
10	EKRPG: selects page of 8K ROM @ >5XXX
11	DMPENA: Start Hardware dump
12	ACK: Acknowledge to SCSI bus, 1 = true
13	INTEN : Enable Interrupt on Sector transfer completed
14	Spare
15	Spare

Input Bit Displacement	Definition	
0	I/O*, Controller driven, (Qualified by REQ)	0 = from Controller to Host 1 = from Host to controller
1	C/D*, Controller driven, (Qualified by REQ)	0 = Data Bytes 1 = Control Bytes
2	MSG, Controller Driven, (Qualified by REQ)	0 = Command is being executed 1 = Command Completed
3	BSY, Controller Driven,	0 = Controller not selected 1 = Controller selected & Ready
4	REQ, Controller Driven Handshake	1 = I/O*, C/D*, MSG are Qualified
5	ACK, Host Adaptor Driven,	1 = Data is accepted or valid
6	CTHRU*, From state counter,	1 = State Counter is active 0 = State Counter is thru
7	Spare	

Figure 3-3 CRU Bit Definitions

3.2.8 Interrupts. The SCSI PCB shall be able to generate an Interrupt to the CPU on completion of a sector transfer if the CRU signal INTEN is set HI. This Interrupt shall be cleared by taking the INTEN signal LO. The interrupt from the SCSI Host Adaptor shall drive Interrupt Level A (ILA*). Interrupt Level

Status Bit (ILSB) 0 shall be driven for the SCSI Host Adaptor interrupt and be used on the Armadillo, but the 99/4A shall not use ILSBs. The ILSA* signal shall be gated to the Data Bus with the LOW true signal "SENILB*".

3.2.9 I/O Voltage Levels. All System Bus signals shall comply with standard TTL voltage levels.

3.2.10 Connectors. The SCSI Host Adaptor Interface connector shall accept a 50-position female ribbon cable connector that consists of two rows of 25 pins on 100 mil centers, 3M #3425-3000 or equivalent, and shall conform to the pin definitions that are listed under I/O PORT DEFINITION.

3.2.11 Cabling. A single 50-conductor ribbon cable will be the only connection necessary between the SCSI Host Adaptor and a SCSI device(intially, the Winchester Disk Subsystem). A slave drive to the master Winchester Disk Subsystem requires a 34-pin cable for control signals and a 20-pin cable for data signals to be run to the Winchester Disk Controller in the master unit. If possible, these 54 conductors will be combined in a single 56-pin cable(which is the next standard size connector/cable) that will in all probability have to be shielded to meet RFI requirements.

3.2.12 SCSI Bus Terminations. The 8 data bus signals of the SCSI bus must be terminated at each end of the SCSI bus with 220 Ohms to
5V, and 330 Ohms to Gnd. These resistors shall be in a standard DIP-type package that is inserted into a socket on the connector tab such that it is user accessible. This is neccesary since only the two devices on each end of the SCSI bus may be terminated. All other devices must not be terminated.

3.2.13 PAL Equation Definitions. The following are the equations necessary for programming the PALs.

PAL 1

```
/FKROM  = V10*/V11*A1*/A3*PCBEN*DBIN*MEMEN*/A4                    (4000-47FF)
         +V10*/V11*A1*/A3*PCBEN*DBIN*MEMEN*/A6*/A7                (44XX,48XX,4CXX)
         +V10*/V11*A1*/A3*PCBEN*DBIN*MEMEN*A4*A5*/A6*A7*/V12      (4D00-4DEF)
         +V10*/V11*A1*/A3*PCBEN*DBIN*MEMEN*A4*/A5                 (4800-4BFF)

/EKROM  = V10*/V11*A1*A3*PCBEN*DBIN*MEMEN*/A4                     (5000-5FFF)

/FKRAM  = V10*/V11*A1*/A3*PCBEN*MEMEN*/A3*A4*A5*A6*A7             (4F00-4FFF)

/OKRAM  = V10*/V11*A1*/A3*PCBEN*MEMEN*/A3*A4*A5*A6*/A7            (4E00-4EFF)

/HDSKEN= V10*/V11*A1*/A3*PCBEN*MEMEN*/A3*A4*A5*/A6*A7*V12         (4E00-4EFF)

/CRUEN  = PCBEN*/MEMEN*/V11*/A1*A3*/A4*/A5*/A6*/A7                (1000-10FF)

        V10 = AMA*AMB*AMC*RPGEN
        V11 = A00 + A02
        V12 = A08*A09*A10*A11
```

PAL 2

```
/BDRVR  = MEMEN*V20*/V11*A1                                       (4000-5FFF)

/FKRWE  = /DMPENA*WE + DMPENA*DMPDIR*RAMR/W

/FKROE  = /DMPENA*DBIN + DMPENA*/DMPDIR

/I/OLTCH = /DMPENA*HDSKEN + /DMPENA*/WE + DMPENA*/ACK

/I/ORD  = DMPENA*I/O- + /DMPENA*HDSKEN*DBIN
```

Figure 3-4 PAL EQUATIONS

3.3 SCSI DEFINITION

The Small Computer System Interface(SCSI) Host Adaptor PCB shall be an interface between the TI 99/4A or ARMADILLO mainframe and a SCSI(or Shugart Associates Standard Interface(SASI) as it was originally defined) compatible peripheral devices. The SCSI is a local I/O bus standard whose primary objective is to provide host computers with a device-independent bus protocal. Therefore, disk drives, tape drives, printers and even communication devices can be added to the host computer without requiring modifications to generic system hardware or software.

3.3.1 Physical Path Specification. The SCSI was specifically designed to provide an efficient method of communication between computers and peripheral input/out devices. SCSI uses an 8-bit data bus with 9 control lines. The spec also provides for :

* Single or multiple host computer system.
* Bus contention handled via distributed-arbitration on a prioritized basis.
* Accommodation of multiple peripheral device types.
* Asynchronous communication of up to an estimated 1.5 MBytes/sec.
* Multiple overlap of peripheral device operations.
* Direct copy between peripheral devices.
* Oriented toward intelligent peripheral devices.

3.3.2 SCSI Bus. Communication on the SCSI Bus is allowed between any two SCSI Bus Ports at any time. There is a maximum of 8 bus ports, with each port connected to a SCSI device. During any communication on the SCSI Bus, one device acts as an INITIATOR(the host computer) and one acts as a TARGET(a peripheral device). Each TARGET may also have up to 8 devices connected to it. In our immediate application, the 99/4A will be the INITIATOR and the Winchester Disk Controller will be the TARGET. This TARGET will be able to control at least 2 peripheral Disks(1 in the same enclosure with the Winchester Disk Controller and 1 in an additional enclosure).

Certain bus functions are assigned to the INITIATOR and certain functions are assigned to the TARGET. The TARGET may request the transfer of COMMAND, DATA, STATUS or other information on the bus, and in some cases it may arbitrate for the bus and reselect an INITIATOR for the purpose of continuing some operation. Data transfers between the two devices are asynchronous and follow a defined 2- wire handshake protocal. One 8-bit byte of information may be transferred with each handshake.

3.3.3 Known 99/4A to Armadillo Incompatibilities. None known at this time.

3.3.4 FCC Compliance. The SCSI Host Adaptor PCB shall comply with Class B limits, Part 15 of FCC rules while functioning normally with a 99/X Home Computer and the TI WinchesterDisk Subsystem.

3.3.5 Test Considerations. Signature Analysis shall be designed in as the primary fault isolation tool, and test specifications for this PCB shall written after both design and prototype debug have been completed.

3.4 WINCHESTER DISK SUBSYSTEM

The Winchester Disk Subsystem to be provided shall consist of a 5 1/4" 6 MByte Winchester Disk(or 12 MByte as an option), an adequate international power supply, a SCSI(single-ended)-compatable Winchester Disk controller, and a suitble enclosure.

3.4.1 Winchester Disk. The Winchester Disk included in the subsystem shall be a 5 1/4" Winchester of 6 MByte or 12 MByte(unformatted).

3.4.2 Power Supply. The power supply included in the subsystem shall be adequate to power the Winchester Disk and any one of the approved SCSI-compatable Winchester Disk Controllers. This same supply shall also be able to be used in the Slave drive subsystem(without controller) with no modifications. This supply shall perform reliably over the entire load range and environmental range.

115VAC, 90VAC to 130 VAC, 47 to 63Hz.
220VAC, 180VAC to 270 VAC, 47 to 63Hz.

Figure 3-5 POWER SUPPLY VOLTAGE RANGES

The power supply shall present to the outside world a standard international 3- prong receptacle to accept international power cords. Units shipped to all U.S. locations shall be configured to 115 VAC and shall include a standard 3-prong grounded power cord. Units shipped to Europe shall be configured to 220 VAC input and shall not include a power cord. Each unit shipped shall have a sticker located near the power receptacle indicating which range the power supply is configured to use.

A VDE, UL, and CSA approved power switch shall be located on the rear of the enclosure. This switch should be the same as used on the Peripheral Expansion System.

3.4.3 Front Panel. The front panel shall have a Power-On indicator and a READ/WRITE indicator. The READ/WRITE indictor shall only be lit when the Winchester Disk Drive is being accessed.

3.4.4 SCSI-Compatible Winchester Disk Controller. The SCSI-Compatible Winchester Disk Controller shall be able to control a minimum of 2 5-1/4" ST-506 compatible Winchester Disk Drives of any combination of 6, 12, or 24 MByte(unformatted) capacity. The controller shall have an ECC scheme to detect and correct single bit errors and flag double bit errors.

SECTION 4

SOFTWARE CHARACTERISTICS

SECTION 5

TEST PLAN

SECTION 6

ENVIRONMENTAL REQUIREMENTS

6.1 TEMPERATURE

6.1.1 Storage.

6.1.2 Operating.

6.2 HUMIDITY

6.2.1 Storage.

6.2.2 Operating.

6.3 ALTITUDE

6.3.1 Storage.

6.3.2 Operating.

6.4 VIBRATION

6.4.1 Storage.

6.4.2 Operating.

SECTION 7

QUALIFICATION

SECTION 8

RELIABILITY

8.1 MTBF GOAL

The MTBF goal shall be 11,000 power on hours.

8.2 MTTR GOAL

The MTTR goal shall be 15 minutes or less.

SECTION 9

MAINTAINABILITY

9.1 SERVICE GOALS

9.2 PHYSICAL SERVICE FEATURES

9.3 REPAIR CENTER SUPPORT PLAN

9.3.1 TECHNIQUES TO BE USED.

9.3.2 DOCUMENTATION TO BE FURNISHED.

9.3.3 EQUIPMENT REQUIRED.

SECTION 10

PHYSICAL REQUIREMENTS

10.1 OUTSIDE DIMENSIONS

10.2 WEIGHT

10.3 AC POWER REQUIREMENTS

10.4 STYLING

SECTION 11

PACKING

SECTION 12

TEST SPECIFICATIONS

SECTION 13

COST REDUCTION PATHS

13.1 GATE ARRAYS/INTEGRATION

SECTION 14

DSG/CPG INTERFACE

SECTION 15

UNIT IDENTIFICATION REQUIREMENTS

15.1 LABEL

SECTION 16

DOCUMENTATION

16.1 USERS MANUAL

SECTION 17

UPDATE TRACKS

APPENDIX

PIN	TYPE	SIGNAL	FUNCTION	GROUND PIN
2	I/O	DATA0/	Data Bus, Bit 0(LSB)	1
4	I/O	DATA1/	Data Bus, Bit 1	3
6	I/O	DATA2/	Data Bus, Bit 2	5
8	I/O	DATA3/	Data Bus, Bit 3	7
10	I/O	DATA4/	Data Bus, Bit 4	9
12	I/O	DATA5/	Data Bus, Bit 5	11
14	I/O	DATA6/	Data Bus, Bit 6	13
16	I/O	DATA7/	Data Bus, Bit 7(MSB)	15
18		SPARE		17
20		SPARE		19
22		SPARE		21
24		SPARE		23
26		SPARE		25
28		SPARE		27
30		SPARE		29
32		SPARE		31
34		SPARE		33
36	received	BUSY/	Controller is ready	35
38	driven	ACK/	Response to REQ/	37
40	driven	RST/	Reset Controller	39
42	received	MSG/	Command completed	41
44	driven	SEL/	Select Controller	43
46	received	C/D	Command/Data	45
48	received	REQ/	Request(start hndshk)	47
50	received	I/O	Input/Output(dir of DIO)	49

Figure 17-1 SCSI BUS PIN-OUT DEFINITION

.100" PIN TO PIN SPACING, PRODUCTION PCBS

PIN #	MNEMONIC	FUNCTION
1		+5V 3-T Regulator supply voltage
2		+5V 3-T Regulator supply voltage
3	GND	Logic Ground
4	READY.A	System READY
5	GND	Logic Ground
6	RESET*	active LOW System driven RESET
7	GND	Logic Ground
8	SCLK	System clock
10	AUDIO	Input audio
11	BDRVREN*	Enable for I/F card buffers
12	PCBEN	active HIGH PCB enable for Burn In
13	HOLD*	Active LOW CPU HOLD request Available on Armadillo only

14	IAQHDA	IAQ HOLDA Logical OR Available on Armadillo only
15	SENILA*	Interrupt Level A Sense Enable
16	SENILB*	Interrupt Level B Sense Enable Used on Armadillo only
17	INTA*	active LOW Interrupt Level A
18	LOAD*	active LOW for TI-99/4 Memory Expansion, High for linear memory space. Second generation C ly CPU LOAD* input
19	D7	System DATA Bus, LSB
20	GND	Logic Ground
21	D5	System DATA Bus
22	D6	System DATA Bus
23	D3	System DATA Bus
24	D4	System DATA Bus
25	D1	System DATA Bus
26	D2	System DATA Bus
27	GND	Logic Ground
28	D0	System DATA Bus, MSB
29	A14.A	Address Bit
30	A15/COUT.A	Address Bit, LSB
31	A12.A	Address Bit
32	A13.A	Address Bit
33	A10.A	Address Bit
34	A11.A	Address Bit
35	A08.A	Address Bit
36	A09.A	Address Bit
37	A06.A	Address Bit
38	A07.A	Address Bit
39	A04.A	Address Bit
40	A05.A	Address Bit
41	A02.A	Address Bit
42	A03.A	Address Bit
43	A00.A	Address Bit, MSB
44	A01.A	Address Bit, normally HIGH
45	AMB.A	Address Bit, normally HIGH
46	AMA.A	Address Bit
47	GND	Logic Ground
48	AMC.A	Address Bit, MSB, normally HIGH
49	GND	Logic Ground
50	CLKOUT*	Active LOW CPU Clock
51	CRUCLK.A*	active LOW CRU Output Clock
52	DBIN.A	Data Bus Dir''tn, HIGH is CPU READ
53	GND	Logic Ground
54	WE.A*	LOW true CPU Write Enable
55	CRUIN	HIGH true CRU Input data
56	MEMEN.A*	active LOW memory request
57		-12V 3-T Regulator supply voltage
58		-12V 3-T Regulator supply voltage

59	+12V 3-T Regulator supply voltage
60	+12V 3-T Regulator supply voltage

Figure 17-2 System Bus I/O Connector Pin Definition

MNEMONIC	DEFINITION
AMC.A	System 19-bit Address Bus MSB
AMB.A	System 19-bit Address Bus
AMA.A	System 19-bit Address Bus
A00.A	System 19-bit Address Bus
A01.A	System 19-bit Address Bus
A02.A	System 19-bit Address Bus
A03.A	System 19-bit Address Bus
A04.A	System 19-bit Address Bus
A05.A	System 19-bit Address Bus
A06.A	System 19-bit Address Bus
A07.A	System 19-bit Address Bus
A08.A	System 19-bit Address Bus
A09.A	System 19-bit Address Bus
A10.A	System 19-bit Address Bus
A11.A	System 19-bit Address Bus
A12.A	System 19-bit Address Bus
A13.A	System 19-bit Address Bus
A14.A	System 19-bit Address Bus
A15/COUT.A	System combination Address Bus LSB and CRU Output Data.
AMC.B	Buffered 19-bit Address Bus MSB
AMB.B	Buffered 19-bit Address Bus
AMA.B	Buffered 19-bit Address Bus
A00.B	Buffered 19-bit Address Bus
A01.B	Buffered 19-bit Address Bus
A02.B	Buffered 19-bit Address Bus
A03.B	Buffered 19-bit Address Bus
A04.B	Buffered 19-bit Address Bus
A05.B	Buffered 19-bit Address Bus
A06.B	Buffered 19-bit Address Bus
A07.B	Buffered 19-bit Address Bus
A08.B	Buffered 19-bit Address Bus
A09.B	Buffered 19-bit Address Bus
A10.B	Buffered 19-bit Address Bus
A11.B	Buffered 19-bit Address Bus
A12.B	Buffered 19-bit Address Bus
A13.B	Buffered 19-bit Address Bus
A14.B	Buffered 19-bit Address Bus
A15/COUT.B	Buffered combination 19-bit Address Bus LSB and CRU Output Data.
BDRVR*	Active Low enable for the Data Bus Bidirectional Bus driver chip (SN74LS245).

CLKOUT.A*	Bus level System Clock. For 99/4A based systems it is the 3 MHz Phase 3 clock. For 99/4B based systems it is a 2.68 MHz clock similar to a 99/4A, but more than twice as wide and a different frequency.
CLKOUT.B*	Buffered System Clock. For 99/4A based systems it is the 3 MHz Phase 3 clock. For 99/4B based systems it is a 2.68 MHz clock similar to a 99/4A, but more than twice as wide and a different frequency.
CRUCLK.A*	System level, Active LOW CRU Clock from the CPU.
CRUCLK.B	Buffered, Active HIGH CRU Clock from the CPU.
CRUCLK.B*	Buffered, Active Low CRU Clock from the CPU.
CRUIN	High True CRU data to the CPU (CRU READ Data).
CRU0*	Active Low enable for a bit CRU operation. It is the CRU base of >01D00
DBIN.B	Buffered, Active Low Data Bus Input control line. The data direction is from the PCB to the CPU when this line is HIGH.
DBIN.B*	Buffered Active Low Data Bus Input control line. The data direction is from the PCB to the CPU when this line is LOW.
DSRROM*	Active Low DSR ROM enable to be ANDed with DBIN.B to drive the DSR ROM Chip Enable pin.
D0	System Side Data Bus MSB
D1	System Side Data Bus
D2	System Side Data Bus
D3	System Side Data Bus
D4	System Side Data Bus
D5	System Side Data Bus
D6	System Side Data Bus
D7	System Side Data Bus LSB
IFC	Interface Clear, sent by the system controller to set the system into a known quiescent state. The system controller becomes the controller in charge.
ILB*	Tristate, Active Low driver for Interrupt Level B.
MEMEN.A*	System Memory Enable control signal from the CPU. When LOW it indicates that a memory access IS required by the CPU. When HIGH it indicates that a CRU MIGHT be taking place.
MEMEN.B*	Buffered Memory Enable control signal from the CPU. When LOW it indicates that a memory access IS required by the CPU. When HIGH it indicates that a CRU MIGHT be taking place.
PCBEN	Active High PCB enable signal. It is used on the Burn In Rack to allow the controlling CPU to talk to only one PCB at a time. When LOW the PCB is disabled for both CRU and Memory operations.
RD0	PCB Side Data Bus MSB
RD1	PCB Side Data Bus
RD2	PCB Side Data Bus
RD3	PCB Side Data Bus

RD4	PCB Side Data Bus
RD5	PCB Side Data Bus
RD6	PCB Side Data Bus
RD7	PCB Side Data Bus LSB
RESET.A*	System Active Low Master Reset line form the CPU.
RESET.B*	Buffered Active Low Master Reset line form the CPU.
RPGEN	Active High DSR ROM Page Bit. It must be HIGH before the DSR ROM may be accessed.
SENILB*	CPU driven line to allow the PCB to gate interrupt data to the system side of the Data Bus.

Fisure 17-3 MNEMONIC DEFINITIONS

1. It appears that the YEAR is stored in RAM. What is the memory location?.

2. Need schematic. Is clock interrupt available?

3. What is the CRU base address of card?

---

128 - 512 K card

>5FEC - E YEAR

MM58274

>1000 - 1F00

compressed
OR
NO compressed

NO

Jumpers Right Lower

>A000 UTILITY NAME LENGTH

>A001 ->A028 UTILITY NAME 40 CHR MAX

>A696 ->A6BD

>A6BE P=1 = File protected, P=0 UNPRO

>A6BF STATUS AFTER EXECUTE 1 OR 2

	MEM IMG FILE UTIL/OBC	MAPDSR/OBC	LOADER COPYF/OBC
VDPBUF	2TYP 0000	0000	0000
[illegible]	2TYP 068E ← Prog length →	050C	08E6
[illegible]	2TYP A000 ← CPU Addr →	A683	A688
[illegible]	2TYP 0000 ← CRUADD 1st exec →	A776	A7A6
VDPBUF+18	2TYP 2078 2nd exec →	A91E	6000

1. Process files with PAB just as if they were on floppy.

2. Directories: INTERNAL, RELATIVE, FIXED

Directory

RECORD NAME$, FT, SIZEAL, RECLEN, CS, CMI, CH, CD, CMO, CYL

ABS(FT) = FILE TYPE

IF FT < 0 THEN FILE IS PROTECTED

IF FT = 6 DIRECTORY

TYPE 1 = DIS/FIX -1 prot

2 = DIS/VAR -2 prot

3 = INT/FIX -3 prot

4 = INT/VAR -4 prot

5 = PROGRAM -5 prot

6 = DIRECTORY -6 prot

FILES

NAME$, FT, SIZEAL, RECLEN, CS, CMI, CH, CD, CMO, CYL,

MS, MMI, MH, MD, MMO, MY1

WDS